REMARKS

Response to §102 and §103 Rejections of Claims 16-18 and 20

In the April 13, 2006 Office Action, the Examiner rejected claims 16-18 and 20 on various reference grounds. Specifically, the Examiner rejected:

- Claim 16 under 35 U.S.C. §102(b) as alleged anticipated by U.S. Patent No. 5,599,726 to Pan (hereinafter "Pan");
- Claims 17-18 under 35 U.S.C. §103(a) as alleged obvious over Pan;
- Claims 16-18 under 35 U.S.C. §103(a) as alleged obvious over the combination of U.S. Patent No. 6,555,829 to Horstman et al. (hereinafter "Horstman") and Pan; and
- Claim 20 under 35 U.S.C. §103(a) as alleged obvious over the combination of Horstman, Pan, and U.S. Patent No. 5,973,371 to Kasai et al. (hereinafter "Kasai").

In response, Applicants have hereby amended claim 16, from which claims 17-18 and 20 depend, to positively recite a MOSFET device that comprises "a silicon substrate having shallow trench isolation STI and source and drain regions located therein, a gate dielectric and a gate stack located on said silicon substrate between the source and drain regions, and a fluorine doped low K dielectric oxide gate spacers located on sidewalls of said gate stack, said fluorine doped low K dielectric oxide gate spacer having a fluorine content of about 1E14 to 2E16 cm^{-2}, wherein the source and drain regions are essentially free of fluorine."

Support for the claim amendment can be found in the instant specification in FIG. 5 and on page 5, paragraph [0022], which describes the use of a HDP oxide layer to block the fluorine and prevent the fluorine from entering the source/drain regions of the silicon substrate during the angled fluorine implantation process. Consequently, the source/drain regions of the resulting MOSFET device are essentially free of fluorine.

Claims 16-18 and 20 as amended herein **concurrently** recites: (1) a fluorine doped low K dielectric oxide gate spacer having a fluorine content of about 1E14 to 2E16 cm^{-2}, **and** (2) source and drain regions that are essentially free of fluorine.

It is important to recognize that formation of such a fluorine doped low K dielectric oxide gate spacer with a fluorine content as high as from about 1E14 to 2E16 cm^{-2}, while concurrently maintaining the source and drain regions essentially free of fluorine, is an advancement achieved by the present invention over the prior art.

The newly cited Pan reference discloses a fluorine-doped oxide spacer 18 having a fluorine content of from about 1E14 to about 1E16 per square centimeter (see Pan, column 6, lines 39-41). The fluorine-doped oxide spacer 18 is formed by a blanket fluorine implantation step (see Pan, Figure 2, and column 6, lines 27-30), during which the source and drain regions 24a and 24b in the substrate 10 are **not protected** from fluorine implantation. Inevitably, a significant amount of fluorine ions are implanted into the source and drain regions 24a and 24b in the substrate 10.

Therefore, **the Pan reference fails to disclose a MOSFET device having "source and drain regions essentially free of fluorine," as positively recited by the amended claims 16-18 and 20 of the present application**.

In contrast, the present invention uses an HDT oxide layer to protect the source and drain regions in the substrate during the angled fluorine implantation, so as to form the high-fluorine-content dielectric oxide gate spacer recited by claims 16-18 and 20, but without introducing fluorine into the source and drain regions.

In the outstanding Office Action, the Examiner has expressly conceded that the Horstman reference does not disclosure a fluorinated dielectric oxide gate spacer with a fluorine content as high as from 1E14 to 2E16 cm^{-2}, but asserted that it would be obvious to combine the disclosure of Horstman and Pan to yield a MOSFET device with a fluorine doped dielectric oxide gate spacer having the high fluorine content as recited by claims 16-18 and 20 of the present application (see Office Action, page 4, last paragraph).

However, the high-fluorine-content dielectric oxide gate spacer 18 disclosed by Pan is formed by a blanket fluorine implantation step, during which fluorine ions are implanted not only into the gate spacer 18, but also into the source and drain regions 24a and 24b in the substrate 10, as explained hereinabove. Therefore, the combination of Horstman and Pan, as proposed by the Examiner, would have yield a MOSFET device comprising not only a fluorinated dielectric oxide gate spacer having a fluorine content from 1E14 to 2E16 cm^{-2}, but also fluorinated source and drain regions. In other words, the proposed combination of

Horstman and Pan still cannot yield the MOSFET device as positively recited by claims 16-18 and 20, i.e., a MOSFET with (1) a fluorine doped low K dielectric oxide gate spacer having a fluorine content of about 1E14 to 2E16 cm^{-2} **and** (2) source and drain regions that are essentially free of fluorine.

Similar to Horstman, the Kasai reference discloses a fluorinated dielectric oxide gate spacer 27, but it fails to disclose the high fluorine content of 1E14 to 2E16 cm^{-2}, as recited by claims 16-18 and 20 of the present application. Correspondingly, the combination of Kasai with Pan also cannot yield the MOSFET device as positively recited by claims 16-18 and 20.

In summary, the cited references Pan, Horstman, and Kasai, either taking singularly or in combination, do not provide any derivative basis for a MOSFET with (1) a fluorine doped low K dielectric oxide gate spacer having a fluorine content of about 1E14 to 2E16 cm^{-2} **and** (2) source and drain regions that are essentially free of fluorine, as positively recited by claims 16-18 and 20 of the present application.

Response to §102 Rejection of Claim 21

In the outstanding Office Action, the Examiner rejected claim 21 under 35 U.S.C. §102(b) as alleged anticipated by Kasai.

In response, Applicants have hereby amended claim 21 to recite a silicon nitride oxide layer that not only overlays the gate stack, but also the remaining surfaces of the silicon substrate. Support for the claim amendment can be found in FIG. 7 of the instant specification, which shows an oxidized silicon nitride etch stop layer that overlays the gate stack as well as the remaining surfaces of the silicon substrate, including the source and drain regions and the STI regions.

The silicon nitride oxide layer 26 disclosed by Kasai only covers the gate electrode 25, but not the remaining surfaces of the substrate 21 (see Kasai, Figure 7). Further, nothing in Kasai teaches or suggests modification of the silicon nitride oxide layer 26.

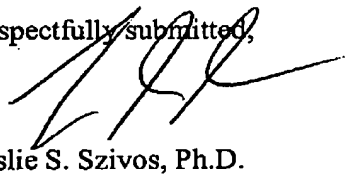
Therefore, the amended claim 21 patentably distinguishes over Kasai, by positively reciting a silicon nitride oxide layer that overlays the gate stack and remaining surfaces of the silicon substrate.

CONCLUSION

Based on the foregoing, Applicants respectfully request the Examiner to reconsider, and upon reconsideration to withdraw, the rejections of claims 16-18 and 20-21 as amended herein and to issue a Notice of Allowance in Applicants' favor.

If any issues remain outstanding, incident to the formal allowance of the application, the Examiner is requested to contact the undersigned at (516) 742-4343 to discuss same, in order that this application may be allowed and passed to issue at an early date.

Respectfully submitted,



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